USER MANUAL

Accessory 21A

PMAC2 JOPTO Part Interface for OPTO 22

3Ax-603375-xUxx

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DELTA TAU
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21314 Lassen Street Chatsworth, CA 91311 // Tel. (818) 998-2095 Fax. (818) 998-7807 // www.deltatau.com

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Delta Tau Data Systems, Inc. Technical Support
Phone: (818) 717-5656
Fax: (818) 998-7807
Email: support@deltatau.com
Website: http://www.deltatau.com

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INTRODUCTION

The ACC-21A was created to give the user the capability to use PMAC2's JOPTO port with OPTO 22 or Grayhill style I/O module racks. The ACC-21A can be used with the 8, 16, 24, or 32 module boards from these manufacturers. The PMAC2 JOPTO port has 32 bits of inputs and outputs that can be software configured as inputs or outputs on a byte-by-byte basis. The following table lists the possible input/out schemes possible with the PMAC2 JOPTO port.

Inputs	Outputs
32	0
24	8
16	16
8	24
0	32

USING THE PMAC2 JOPTO PORT

The 32 I/O lines are memory-mapped into PMAC's address space in registers Y:$C080 and Y:$C081 for PMAC2 and Y:$78400 and Y:$78401 for Turbo PMAC2. Typically these I/O lines are accessed individually with M-variables. Following is a suggested set of M-variable definitions to use these data lines:

PMAC2	Turbo PMAC2	Description
M0->Y:$C080,0	M0->Y:$78400,0	I/O00 Data Line J3 Pin 1
M1->Y:$C080,1	M1->Y:$78400,1	I/O01 Data Line J3 Pin 2
M2->Y:$C080,2	M2->Y:$78400,2	I/O02 Data Line J3 Pin 3
M3->Y:$C080,3	M3->Y:$78400,3	I/O03 Data Line J3 Pin 4
M4->Y:$C080,4	M4->Y:$78400,4	I/O04 Data Line J3 Pin 5
M5->Y:$C080,5	M5->Y:$78400,5	I/O05 Data Line J3 Pin 6
M6->Y:$C080,6	M6->Y:$78400,6	I/O06 Data Line J3 Pin 7
M7->Y:$C080,7	M7->Y:$78400,7	I/O07 Data Line J3 Pin 8
M8->Y:$C080,8	M8->Y:$78400,8	I/O08 Data Line J3 Pin 9
M9->Y:$C080,9	M9->Y:$78400,9	I/O09 Data Line J3 Pin 10
M10->Y:$C080,10	M10->Y:$78400,10	I/O10 Data Line J3 Pin 11
M11->Y:$C080,11	M11->Y:$78400,11	I/O11 Data Line J3 Pin 12
M12->Y:$C080,12	M12->Y:$78400,12	I/O12 Data Line J3 Pin 13
M13->Y:$C080,13	M13->Y:$78400,13	I/O13 Data Line J3 Pin 14
M14->Y:$C080,14	M14->Y:$78400,14	I/O14 Data Line J3 Pin 15
M15->Y:$C080,15	M15->Y:$78400,15	I/O15 Data Line J3 Pin 16
M16->Y:$C080,16	M16->Y:$78400,16	I/O16 Data Line J3 Pin 17
M17->Y:$C080,17	M17->Y:$78400,17	I/O17 Data Line J3 Pin 18
M18->Y:$C080,18	M18->Y:$78400,18	I/O18 Data Line J3 Pin 19
M19->Y:$C080,19	M19->Y:$78400,19	I/O19 Data Line J3 Pin 20
M20->Y:$C080,20	M20->Y:$78400,20	I/O20 Data Line J3 Pin 21
M21->Y:$C080,21	M21->Y:$78400,21	I/O21 Data Line J3 Pin 22
M22->Y:$C080,22	M22->Y:$78400,22	I/O22 Data Line J3 Pin 23
M23->Y:$C080,23	M23->Y:$78400,23	I/O23 Data Line J3 Pin 24
M24->Y:$C081,0	M24->Y:$78401,0	I/O24 Data Line J3 Pin 25
M25->Y:$C081,1	M25->Y:$78401,1	I/O25 Data Line J3 Pin 26
M26->Y:$C081,2	M26->Y:$78401,2	I/O26 Data Line J3 Pin 27
M27->Y:$C081,3	M27->Y:$78401,3	I/O27 Data Line J3 Pin 28
M28->Y:$C081,4	M28->Y:$78401,4	I/O28 Data Line J3 Pin 29
M29->Y:$C081,5	M29->Y:$78401,5	I/O29 Data Line J3 Pin 30
M30->Y:$C081,6	M30->Y:$78401,6	I/O30 Data Line J3 Pin 31
M31->Y:$C081,7	M31->Y:$78401,7	I/O31 Data Line J3 Pin 32

DIRECTION CONTROL

The PMAC2 JIO direction control is used to setup the I/O bytes as either inputs or outputs. The direction control bit for each of these I/O bits is in the corresponding bit in the matching X register. For example, the direction control bit for I/O03 is located at X:$C080,3 and X:$78400,3 for Turbo PMAC2; the direction control bit for I/O30 is located at X:$C081,6 and X:$78401,6 for Turbo PMAC2. Because the buffer ICs can only be switched by byte, it is best to define 8-bit M-variables for the direction control. Suggested definitions are:

PMAC2	Turbo PMAC2	Description
`M32->X:$C080,0,8`	`M32->X:$78400,0,8`	Direction control for I/O00 to I/O07
`M34->X:$C080,8,8`	`M34->X:$78400,8,8`	Direction control for I/O08 to I/O15
`M36->X:$C080,16,8`	`M36->X:$78400,16,8`	Direction control for I/O16 to I/O23
`M38->X:$C081,0,8`	`M38->X:$78401,0,8`	Direction control for I/O24 to I/O31

These M-variables should take values of 0 or 255 ($FF) only; **0** sets the byte to **input**, **255** sets the byte to **output**.

In addition, the bi-directional buffer IC for each byte has a direction control line accessible as a software control bit. These control lines and bits must match the ASIC direction bits. The buffer direction control bits are at PMAC address Y:$E800 or Y:$70800, with bits 0 to 3 controlling the four bytes of the JIO port. A bit value of **0** specifies **input; 1** specifies **output**. Suggested M-variable definitions are:

PMAC2	Turbo PMAC2	Description
`M33->Y:$E800,0`	`M33->Y:$70800,0`	Buffer direction control for I/O00 to I/O07
`M35->Y:$E800,1`	`M35->Y:$70800,1`	Buffer direction control for I/O08 to I/O15
`M37->Y:$E800,2`	`M37->Y:$70800,2`	Buffer direction control for I/O16 to I/O23
`M39->Y:$E800,3`	`M39->Y:$70800,3`	Buffer direction control for I/O24 to I/O31

In the default configuration automatically set at power-up/reset, I/O00 to I/O31 are set up as inputs (M882 through M889 = 0). This is done for maximum safety; no lines can be forced into an undesirable high or low state. Any of these lines that are to be used as outputs must be changed to outputs by user programs (usually this is done in PLC 1 acting as a "reset" PLC, scanning through once on power-up/reset, then disabling itself).

INVERSION CONTROL

Each line on the JIO port is individually controllable as to whether it is an inverting I/O point (0=+5V; 1=0V) or a non-inverting I/O point (0=0V; 1=+5V).

PMAC2	Turbo PMAC2	Description
M80->X:$C084,0,24	M80->X:$78404,0,24	Inversion control for bits 0 to 23
M81->X:$C085,0,8	M81->X:$78405,0,8	Inversion control for bits 24 to 31

A value of 0 in the control bit sets the corresponding I/O point as non-inverting. A value of 1 in the control bits sets the corresponding I/O point as inverting. At power-up/reset, PMAC automatically sets all of the I/O points on the JIO port as non-inverting.

ALTERNATE USES

Each general-purpose I/O point on the JIO port has an alternate use as a supplemental fixed-use I/O point on a supplemental machine interface channel (1* or 2*). The points are individually controllable as to general-purpose use or fixed use by control registers Y:$C084 and Y:$C085. Refer to these registers in the memory-I/O map to see the alternate uses of each point. At power-up/reset, PMAC2 automatically sets up all of the I/O points on the port for general-purpose use.

Note:

The direction-control of the buffer ICs must be set properly for the alternate uses of the I/O points, just as for the general-purpose I/O uses.

EXAMPLE SETUP

For this example we will setup the first 2 bytes of the JIO port as outputs and the last two bytes will be setup as inputs. We also would like the logic for all inputs and outputs to be non-inverting (0=0V; 1=+5V).

```
#define     JIO_OUT_0         M0
#define     JIO_OUT_1         M1
#define     JIO_OUT_2         M2
#define     JIO_OUT_3         M3
#define     JIO_OUT_4         M4
#define     JIO_OUT_5         M5
#define     JIO_OUT_6         M6
#define     JIO_OUT_7         M7
#define     JIO_OUT_8         M8
#define     JIO_OUT_9         M9
#define     JIO_OUT_10        M10
#define     JIO_OUT_11        M11
#define     JIO_OUT_12        M12
#define     JIO_OUT_13        M13
#define     JIO_OUT_14        M14
#define     JIO_OUT_15        M15
#define     JIO_IN_0          M16
#define     JIO_IN_1          M17
#define     JIO_IN_2          M18
#define     JIO_IN_3          M19
#define     JIO_IN_4          M20
#define     JIO_IN_5          M21
#define     JIO_IN_6          M22
#define     JIO_IN_7          M23
#define     JIO_IN_8          M24
#define     JIO_IN_9          M25
#define     JIO_IN_10         M26
#define     JIO_IN_11         M27
#define     JIO_IN_12         M28
#define     JIO_IN_13         M29
#define     JIO_IN_14         M30
#define     JIO_IN_15         M31
#define     DIR_CONTROL_1     M32
#define     BUF_CONTROL_1     M33
#define     DIR_CONTROL_2     M34
#define     BUF_CONTROL_2     M35
#define     DIR_CONTROL_3     M36
#define     BUF_CONTROL_3     M37
#define     DIR_CONTROL_4     M38
#define     BUF_CONTROL_4     M39
#define     INV_CTRL_0_23     M80
#define     INV_CTRL_24_31    M81
M0->Y:$C080,0      ; I/O00 Data Line; J3 Pin 1
M1->Y:$C080,1      ; I/O01 Data Line; J3 Pin 2
M2->Y:$C080,2      ; I/O02 Data Line; J3 Pin 3
M3->Y:$C080,3      ; I/O03 Data Line; J3 Pin 4
M4->Y:$C080,4      ; I/O04 Data Line; J3 Pin 5
```

```
M5->Y:$C080,5     ; I/O05 Data Line; J3 Pin 6
M6->Y:$C080,6     ; I/O06 Data Line; J3 Pin 7
M7->Y:$C080,7     ; I/O07 Data Line; J3 Pin 8
M8->Y:$C080,8     ; I/O08 Data Line; J3 Pin 9
M9->Y:$C080,9     ; I/O09 Data Line; J3 Pin 10
M10->Y:$C080,10   ; I/O10 Data Line; J3 Pin 11
M11->Y:$C080,11   ; I/O11 Data Line; J3 Pin 12
M12->Y:$C080,12   ; I/O12 Data Line; J3 Pin 13
M13->Y:$C080,13   ; I/O13 Data Line; J3 Pin 14
M14->Y:$C080,14   ; I/O14 Data Line; J3 Pin 15
M15->Y:$C080,15   ; I/O15 Data Line; J3 Pin 16
M16->Y:$C080,16   ; I/O16 Data Line; J3 Pin 17
M17->Y:$C080,17   ; I/O17 Data Line; J3 Pin 18
M18->Y:$C080,18   ; I/O18 Data Line; J3 Pin 19
M19->Y:$C080,19   ; I/O19 Data Line; J3 Pin 20
M20->Y:$C080,20   ; I/O20 Data Line; J3 Pin 21
M21->Y:$C080,21   ; I/O21 Data Line; J3 Pin 22
M22->Y:$C080,22   ; I/O22 Data Line; J3 Pin 23
M23->Y:$C080,23   ; I/O23 Data Line; J3 Pin 24
M24->Y:$C081,0    ; I/O24 Data Line; J3 Pin 25
M25->Y:$C081,1    ; I/O25 Data Line; J3 Pin 26
M26->Y:$C081,2    ; I/O26 Data Line; J3 Pin 27
M27->Y:$C081,3    ; I/O27 Data Line; J3 Pin 28
M28->Y:$C081,4    ; I/O28 Data Line; J3 Pin 29
M29->Y:$C081,5    ; I/O29 Data Line; J3 Pin 30
M30->Y:$C081,6    ; I/O30 Data Line; J3 Pin 31
M31->Y:$C081,7    ; I/O31 Data Line; J3 Pin 32
M32->X:$C080,0,8  ; Direction control for I/O00 to I/O07
M34->X:$C080,8,8  ; Direction control for I/O08 to I/O15
M36->X:$C080,16,8 ; Direction control for I/O16 to I/O23
M38->X:$C081,0,8  ; Direction control for I/O24 to I/O31
M33->Y:$E800,0    ; Buffer direction control for I/O00 to I/O07
M35->Y:$E800,1    ; Buffer direction control for I/O08 to I/O15
M37->Y:$E800,2    ; Buffer direction control for I/O16 to I/O23
M39->Y:$E800,3    ; Buffer direction control for I/O24 to I/O31
M80->X:$C084,0,24 ; Inversion control for bits 0 to 23
M81->X:$C085,0,8  ; Inversion control for bits 24 to 31
```

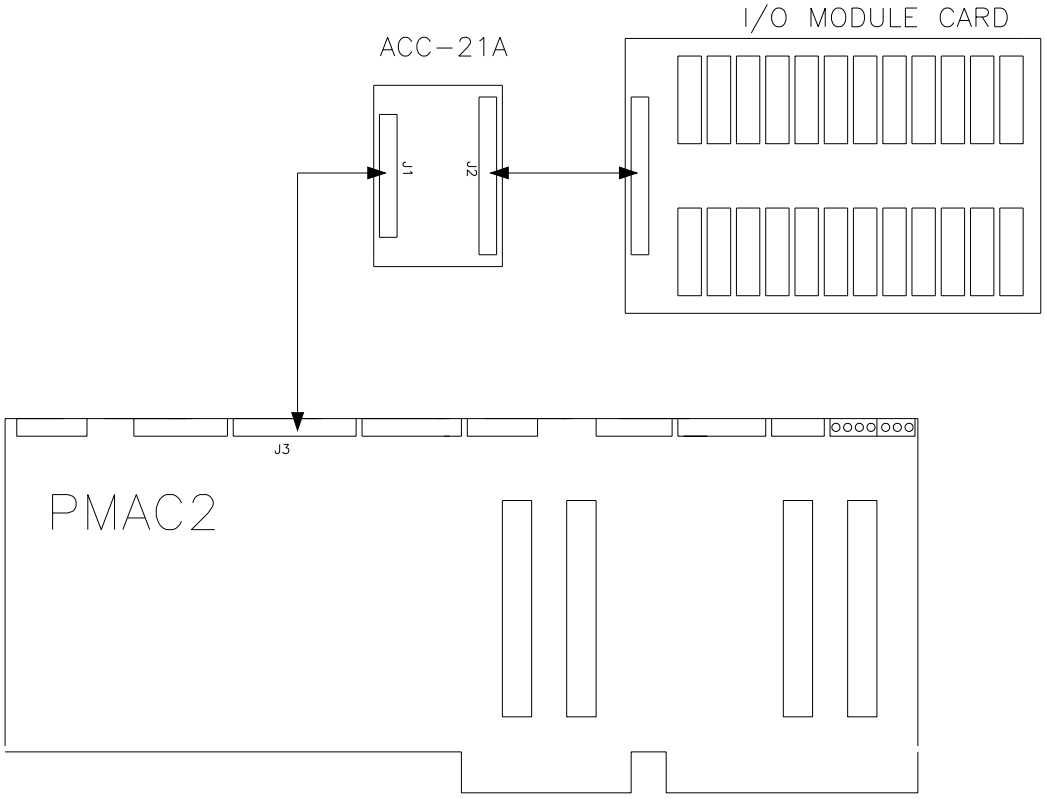
If the above definitions were made, we could set these variables to their proper values in an initialization PLC. I usually will use the following technique for an initialization PLC,

```
OPEN PLC 6 CLEAR
DIR_CONTROL_1 = 255        ;set as output
BUF_CONTROL_1 = 1          ;set as output
DIR_CONTROL_2 = 255        ;set as output
BUF_CONTROL_2 = 1          ;set as output
DIR_CONTROL_3 = 0          ;set as input
BUF_CONTROL_3 = 0          ;set as input
DIR_CONTROL_4 = 0          ;set as input
BUF_CONTROL_4 = 0          ;set as input
INV_CTRL_0_23 = 0          ;set as non-inverting
INV_CTRL_24_31 =0          ;set as non-inverting
```

```
;place other initialization variables here
while (1<2)
.
.          ;PLC in here (perhaps E_STOP routine)
.
.
endwhile
```
CLOSE

Using this technique, we will have a one-time read of the initialization variables used by the card and the logic for the PLCs.

ACC-21A SETUP DIAGRAM



J1 – 40 PIN INPUT FROM PMAC2 JOPTO

Pin #	Symbol	Function	Description	Notes
1	I/O00	I/O	Digital I/O 0	Software Direction Control
2	I/O01	I/O	Digital I/O 1	Software Direction Control
3	I/O02	I/O	Digital I/O 2	Software Direction Control
4	I/O03	I/O	Digital I/O 3	Software Direction Control
5	I/O04	I/O	Digital I/O 4	Software Direction Control
6	I/O05	I/O	Digital I/O 5	Software Direction Control
7	I/O06	I/O	Digital I/O 6	Software Direction Control
8	I/O07	I/O	Digital I/O 7	Software Direction Control
9	I/O08	I/O	Digital I/O 8	Software Direction Control
10	I/O09	I/O	Digital I/O 9	Software Direction Control
11	I/O10	I/O	Digital I/O 10	Software Direction Control
12	I/O11	I/O	Digital I/O 11	Software Direction Control
13	I/O12	I/O	Digital I/O 12	Software Direction Control
14	I/O13	I/O	Digital I/O 13	Software Direction Control
15	I/O14	I/O	Digital I/O 14	Software Direction Control
16	I/O15	I/O	Digital I/O 15	Software Direction Control
17	I/O16	I/O	Digital I/O 16	Software Direction Control
18	I/O17	I/O	Digital I/O 17	Software Direction Control
19	I/O18	I/O	Digital I/O 18	Software Direction Control
20	I/O19	I/O	Digital I/O 19	Software Direction Control
21	I/O20	I/O	Digital I/O 20	Software Direction Control
22	I/O21	I/O	Digital I/O 21	Software Direction Control
23	I/O22	I/O	Digital I/O 22	Software Direction Control
24	I/O23	I/O	Digital I/O 23	Software Direction Control
25	I/O24	I/O	Digital I/O 24	Software Direction Control
26	I/O25	I/O	Digital I/O 25	Software Direction Control
27	I/O26	I/O	Digital I/O 26	Software Direction Control
28	I/O27	I/O	Digital I/O 27	Software Direction Control
29	I/O28	I/O	Digital I/O 28	Software Direction Control
30	I/O29	I/O	Digital I/O 29	Software Direction Control
31	I/O30	I/O	Digital I/O 30	Software Direction Control
32	I/O31	I/O	Digital I/O 31	Software Direction Control
33	GND	Common	Ref. Voltage	
34	GND	Common	Ref. Voltage	
35	PHASE/	Output	Phase Clock	For latching data
36	SERVO/	Output	Servo Clock	For latching data
37	GND	Common	Ref. Voltage	
38	GND	Common	Ref. Voltage	
39	+5V	Output	Supply Digital Voltage	To power ext. circuitry
40	+5V	Output	Supply Voltage	To power ext. circuitry
The JI/O connector provides 32 input/output pins at TTL levels. Direction can be controlled in byte-wide groups.				

J2 – 50 PIN BREAKOUT TO I/O MODULE CARD

Pin #	Symbol	Function	Description	Notes
1	IN/OUT23	I/O	Port A Bit 23	User Defined I/O
2	IN/OUT24	I/O	Port A Bit 24	User Defined I/O
3	IN/OUT22	I/O	Port A Bit 22	User Defined I/O
4	IN/OUT25	I/O	Port A Bit 25	User Defined I/O
5	IN/OUT21	I/O	Port A Bit 21	User Defined I/O
6	IN/OUT26	I/O	Port A Bit 26	User Defined I/O
7	IN/OUT20	I/O	Port A Bit 20	User Defined I/O
8	IN/OUT27	I/O	Port A Bit 27	User Defined I/O
9	IN/OUT19	I/O	Port A Bit 19	User Defined I/O
10	IN/OUT28	I/O	Port A Bit 28	User Defined I/O
11	IN/OUT18	I/O	Port A Bit 18	User Defined I/O
12	IN/OUT29	I/O	Port A Bit 29	User Defined I/O
13	IN/OUT17	I/O	Port A Bit 17	User Defined I/O
14	IN/OUT30	I/O	Port A Bit 30	User Defined I/O
15	IN/OUT16	I/O	Port A Bit 16	User Defined I/O
16	IN/OUT31	I/O	Port A Bit 31	User Defined I/O
17	IN/OUT15	I/O	Port A Bit 15	User Defined I/O
18	GND	Common	Opto Common	
19	IN/OUT14	I/O	Port A Bit 14	User Defined I/O
20	GND	Common	Opto Common	
21	IN/OUT13	I/O	Port A Bit 13	User Defined I/O
22	GND	Common	Opto Common	
23	IN/OUT12	I/O	Port A Bit 12	User Defined I/O
24	GND	Common	Opto Common	
25	IN/OUT11	I/O	Port A Bit 11	User Defined I/O
26	GND	Common	Opto Common	
27	IN/OUT10	I/O	Port A Bit 10	User Defined I/O
28	GND	Common	Opto Common	
29	IN/OUT9	I/O	Port A Bit 9	User Defined I/O
30	GND	Common	Opto Common	
31	IN/OUT8	I/O	Port A Bit 8	User Defined I/O
32	GND	Common	Opto Common	
33	IN/OUT7	I/O	Port A Bit 7	User Defined I/O
34	GND	Common	Opto Common	
35	IN/OUT6	I/O	Port A Bit 6	User Defined I/O
36	GND	Common	Opto Common	
37	IN/OUT5	I/O	Port A Bit 5	User Defined I/O
38	GND	Common	Opto Common	
39	IN/OUT4	I/O	Port A Bit 4	User Defined I/O
40	GND	Common	Opto Common	
41	IN/OUT3	I/O	Port A Bit 3	User Defined I/O
42	GND	Common	Opto Common	
43	IN/OUT2	I/O	Port A Bit 2	User Defined I/O
44	GND	Common	Opto Common	
45	IN/OUT1	I/O	Port A Bit 1	User Defined I/O
46	GND	Common	Opto Common	
47	IN/OUT0	I/O	Port A Bit 0	User Defined I/O
48	GND	Common	Opto Common	
49	A +5V	Output	+5 V supply	
50	GND	Common	Opto Common	